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The concept of a Bonded Field-Effect Transistor has been successfully demonstrated, using an InGaAs/InAlAs MESFET Source/Gate region with an InGaN/GaN drain region. Bonding other material combinations such as Si-GaP and Si-GaN have been attempted and explored. Material non-uniformity severely impacts the ability of GaN to bond, and several process developments have been made to attempt to overcome this issue. Many possibilities exist for the continued exploration of this new class of devices, promising both high-frequency and high-voltage operation.

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End of Project Report

AFOSR Wafer Bonding

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Summary

The concept of a Bonded Field-Effect Transistor has been successfully demonstrated, using an InGaAs/InAlAs MESFET Source/Gate region with an InGaN/GaN drain region. Bonding other material combinations such as Si-GaP and Si-GaN have been attempted and explored. Material non-uniformity severely impacts the ability of GaN to bond, and several process developments have been made to attempt to overcome this issue. Many possibilities exist for the continued exploration of this new class of devices, promising both high-frequency and high-voltage operation.

Background

The goal of this project was to produce a Field-Effect Transistor (FET) utilizing and electrically-active wafer-bonded junction. Wafer bonding allows two very dissimilar materials that cannot be grown heteroepitaxially on top of each other, to be joined.

Historically, device design has progressed through a variety of material structures, including:

- Homojunction devices, in Si, using only one material
- Heterojunction devices, in InGaAs/InAlAs, using two or more materials with very similar lattice constants
- Pseudomorphic devices, in AlGaN/GaN, using two or more materials with dissimilar lattice constants and strained, but non-defective material

The next logical progression in this trend is bonded devices, where two materials that cannot be grown pseudomorphically are combined to produce a single structure.

Combining material systems allows the creation of an ideal device, where any material can now be picked for inclusion in the device design. An ideal device would be able to operate at high voltages and high frequencies. However, high-speed materials such as InGaAs tend to have low breakdown voltages, and high-breakdown materials such as GaN tend to be slower (see Figure 1). Luckily, the region of a FET where the voltage peaks is not impacted by low electron velocity, nor are fields particularly high in the regions where velocity is important. Therefore, via bonding, a device can now be designed to include a high-speed electron injector with a high-voltage electron collector, avoiding the downsides of respective materials.

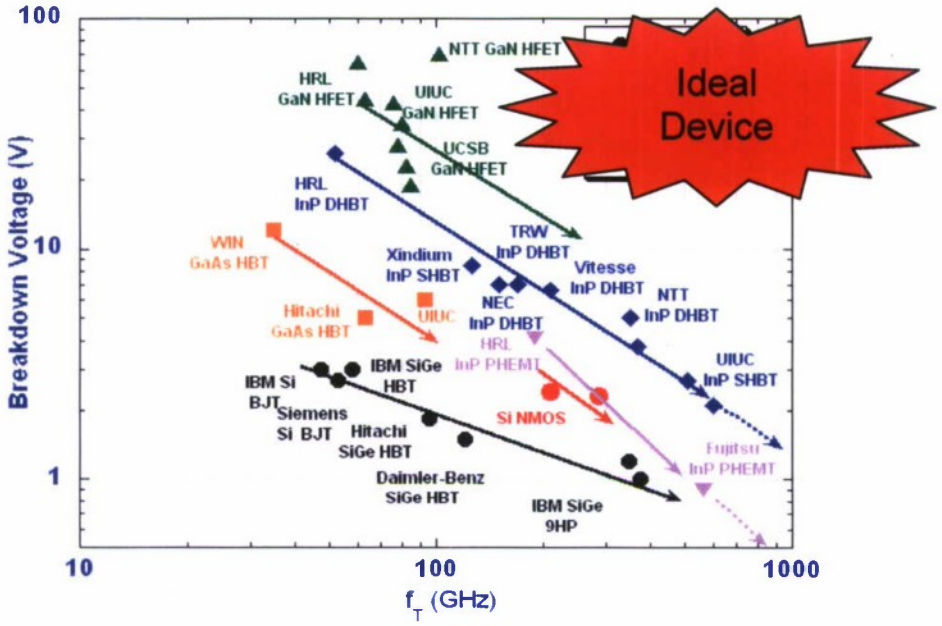


Figure 1
Breakdown vs Ft. Note that breakdown voltage decreases montonically with increasing Ft.

Successes

InGaAs/GaN BAVET

The InGaAs/GaN BAVET (Bonded Aperture Vertical Electron Transistor) is a device modeled on the AlGaN/GaN CAVET, but rather than regrowing an AlGaN/GaN HEMT atop a GaN template, an InGaAs/InAlAs MESFET (or HEMT) is bonded on. We have successfully demonstrated the concept of the BAVET, though it is limited by parasitic currents.

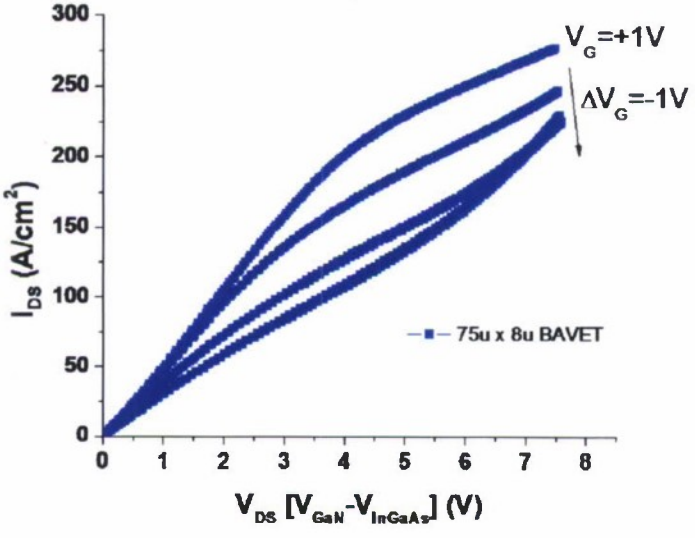


Figure 2
InGaAs-GaN BAVET IV. Gate leakage and high Ron are problematic.

The device consists of the following:

- Burried n-GaN drain
- Current blocking layers
- Small conductive aperture
- Bonded InGaAs-InAlAs MESFET on top.

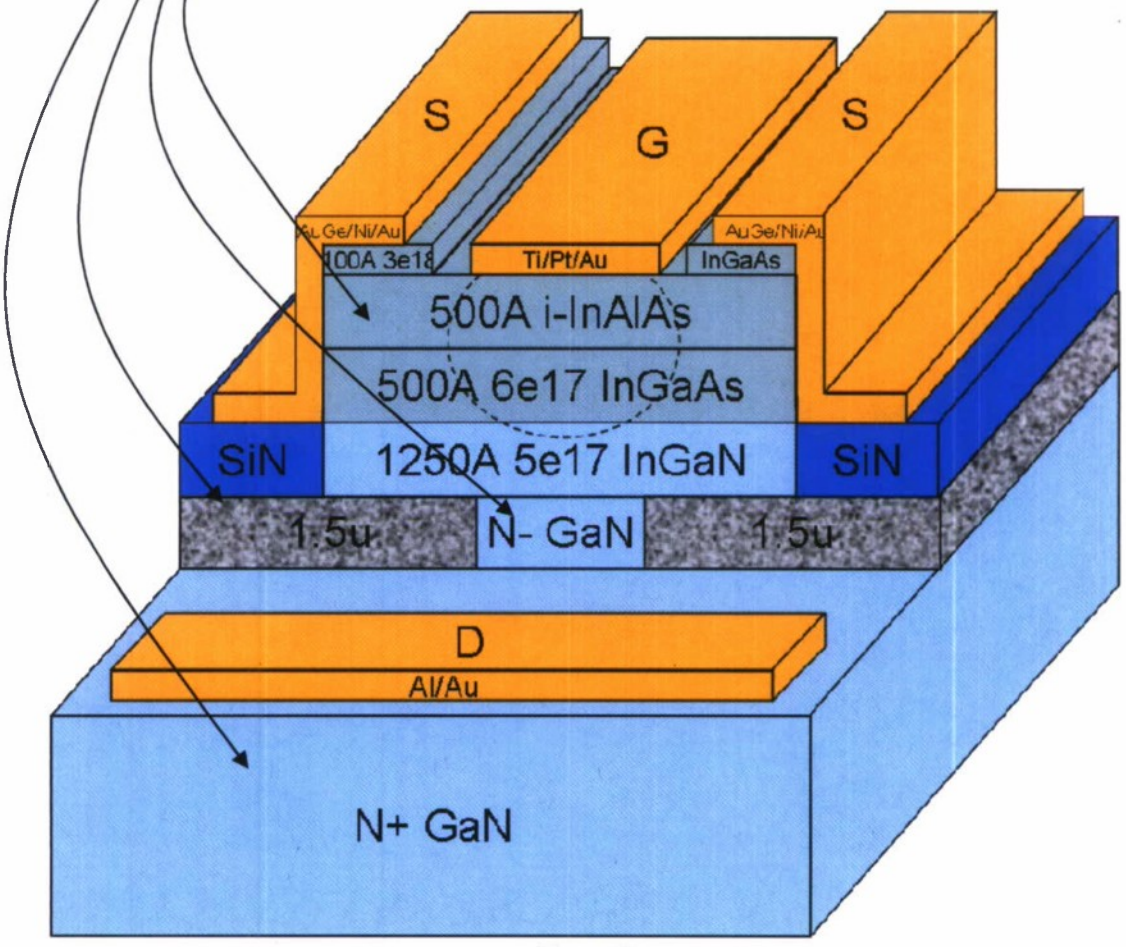


Figure 3
BAVET Structure.
SiN was added to help insulate the source ohmics.

Si/GaP Si/GaN iodes

Silicon integration with compound semiconductors via bonding would open a very large space of new devices, allowing the vast amount of knowledge and capacity of VLSI processes to be integrated and utilized along with GaN.

Because of difficulties in getting Si to bond to GaN, GaP was selected as a precursor to using GaN because of its relatively high band-gap (2.3eV) and the availability of smooth, polished material. Wafer flatness is critical to success in bonding, and it was found that Si and GaP bond readily.

p-Si to n-GaP diodes were constructed, and found to exhibit very good characteristics and followed as one would expect from the material parameters.

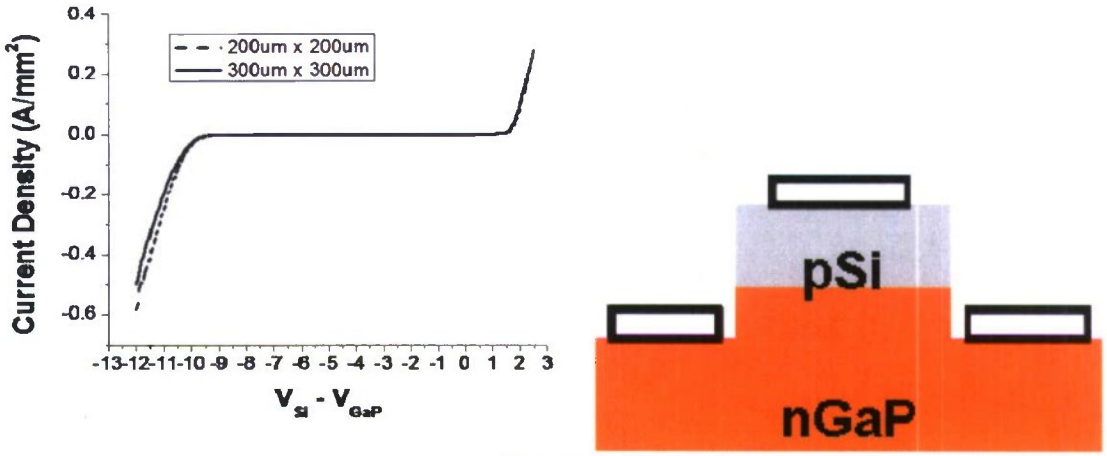


Figure 4
IV data for pSi-nGaP diodes. Reverse leakage and turn on voltage is favorable.

This is the type of structure desirable for making a bonded N-MOSFET, but when we examine the electron flow in an nSi-nGaP diode, it is found that there is a significant barrier to electron transport, as seen in InP-GaN and InGaAs-GaN as well (see section "Electron Barrier" on page 6).

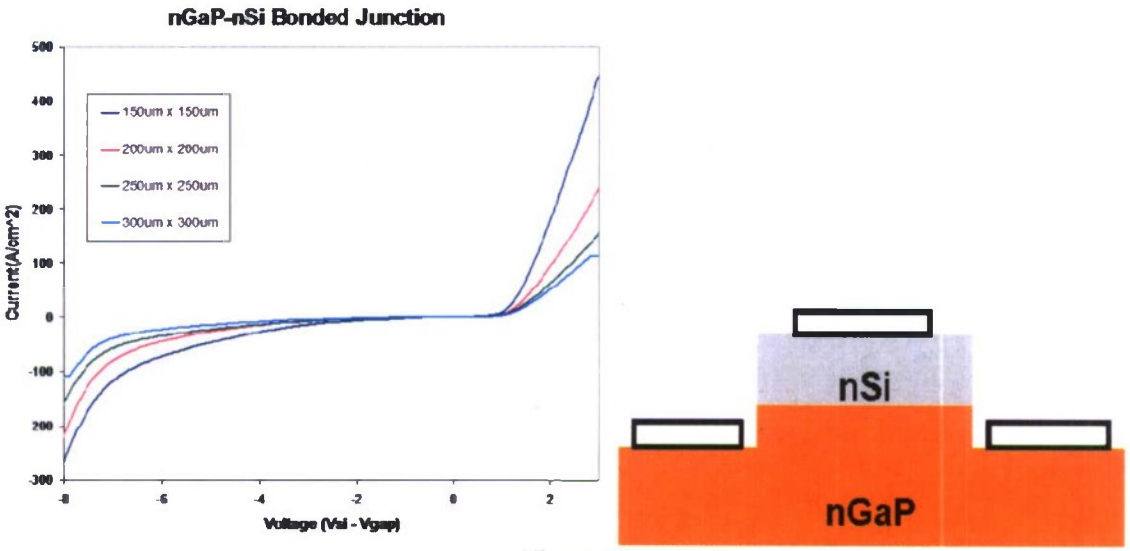


Figure 5
IV data for nSi-nGaP diodes. Behavior is suggestive a very large electron barrier.

Finally, with the availability of MBE-grown GaN suitable for bonding, the first nSi-nGaN diodes were produced. As expected, these too exhibit a large conduction band barrier.

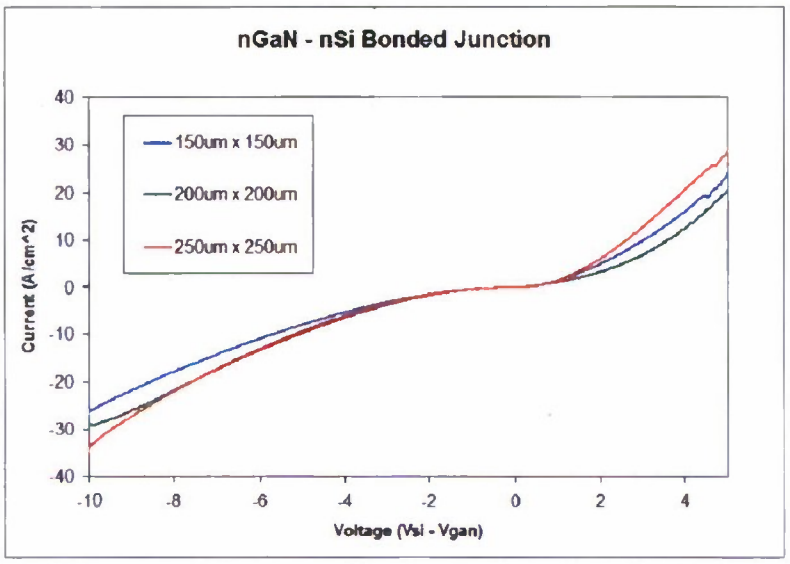


Figure
IV data for nSi-nGaN bond. Structure is similar to that shown in Figure .

Difficulties and Knowledge Added

Surface Morphology and Particles

One of the most important features of materials in determining whether they will bond is the quality of the bonding surfaces, in both cleanliness (foreign particles) and surface morphology (roughness). Two silicon wafers, when properly cleaned, can easily bond at room temperature because of their smooth, polished surface. However, Ga-face GaN does not polish well and the as-grown samples feature step-growth patterns and other micro- and macro-scale nonuniformities.

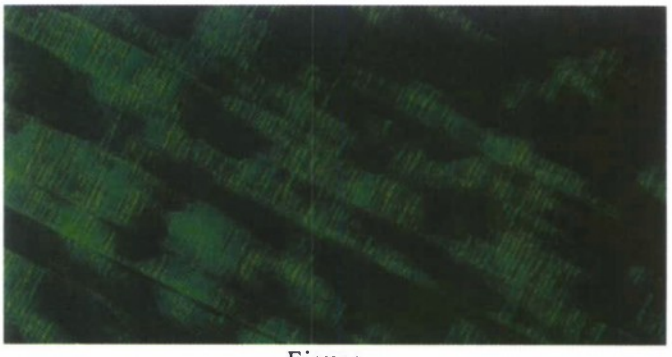


Figure
The roughness in the surface of the GaN leaves voids (light regions) when bonded.

In order to best avoid these issues, a specialized program was developed to control the bonding conditions. A combination a two factors, a stepped temperature/pressure profile and a higher overall pressure, helped to eliminate the voids.

The growth of InGaN on top of GaN proved a particularly problematic issue for bonding. If the InGaN layer is too thin, the piezoelectric charge depletes it of carriers,

and as it has a very low mobility (~80), thick layers are undesirable. Further, the surface morphology is sensitive to a multitude of factors, and very different outcomes exist.

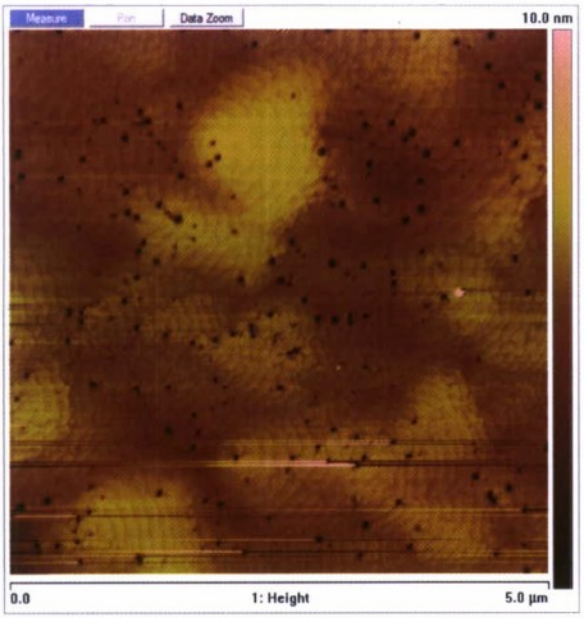


Figure 8
AFM of InGaN shows steps and pits, with light roughness. Bonds well.

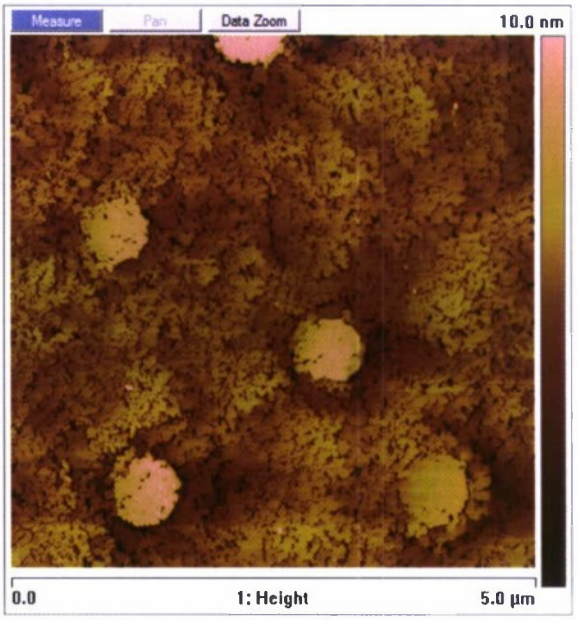


Figure 9
AFM of InGaN shows no steps, excessive pitting and heavy roughness. Does not bond.

Electron Barrier

The next big issue to overcome, once a strong physical bond is made, is electron transport through the junction. As predicted in mathematical models, the I-V characteristics suggest there is a non-negligible electron barrier at the interface. In order to combat this issue, the conduction band discontinuity must be reduced. This can be accomplished by incorporating InGaN in the structure, lowering the discontinuity and improving the current.

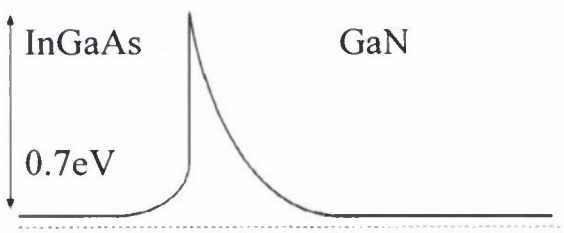


Figure 10
Suggested band structure of InGaAs-GaN bond.

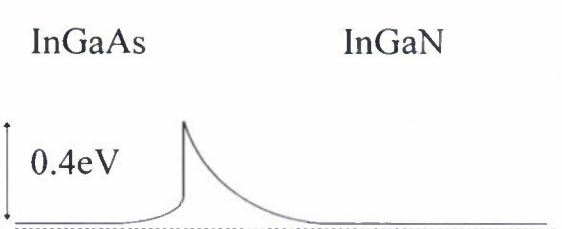
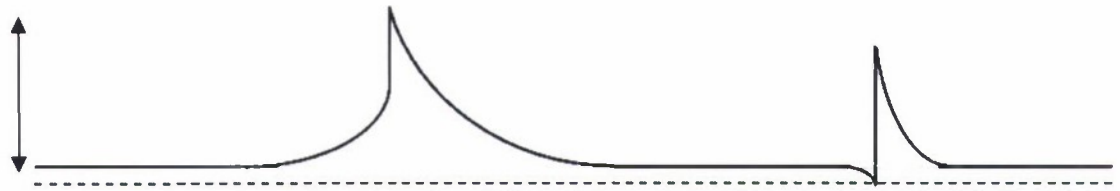


Figure 11
Suggested band structure of InGaAs- $In_{.10}Ga_{.90}N$ bond, with smaller barrier.

Due to the very low mobility of the InGaN, it is undesirable to contact it directly. Therefore, a buried N+ GaN contact is used. The final band diagram is as follows:



Figure

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